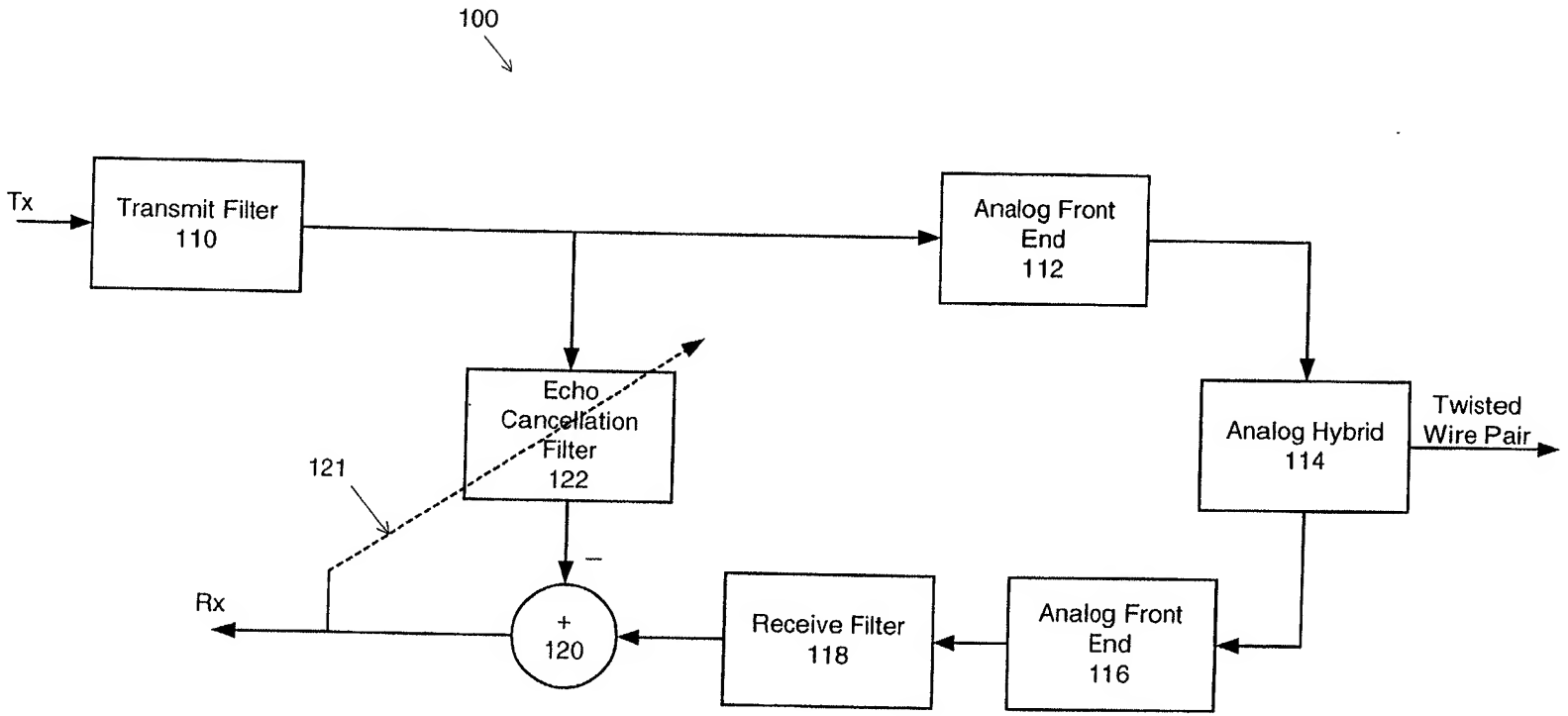


FIG. 1a

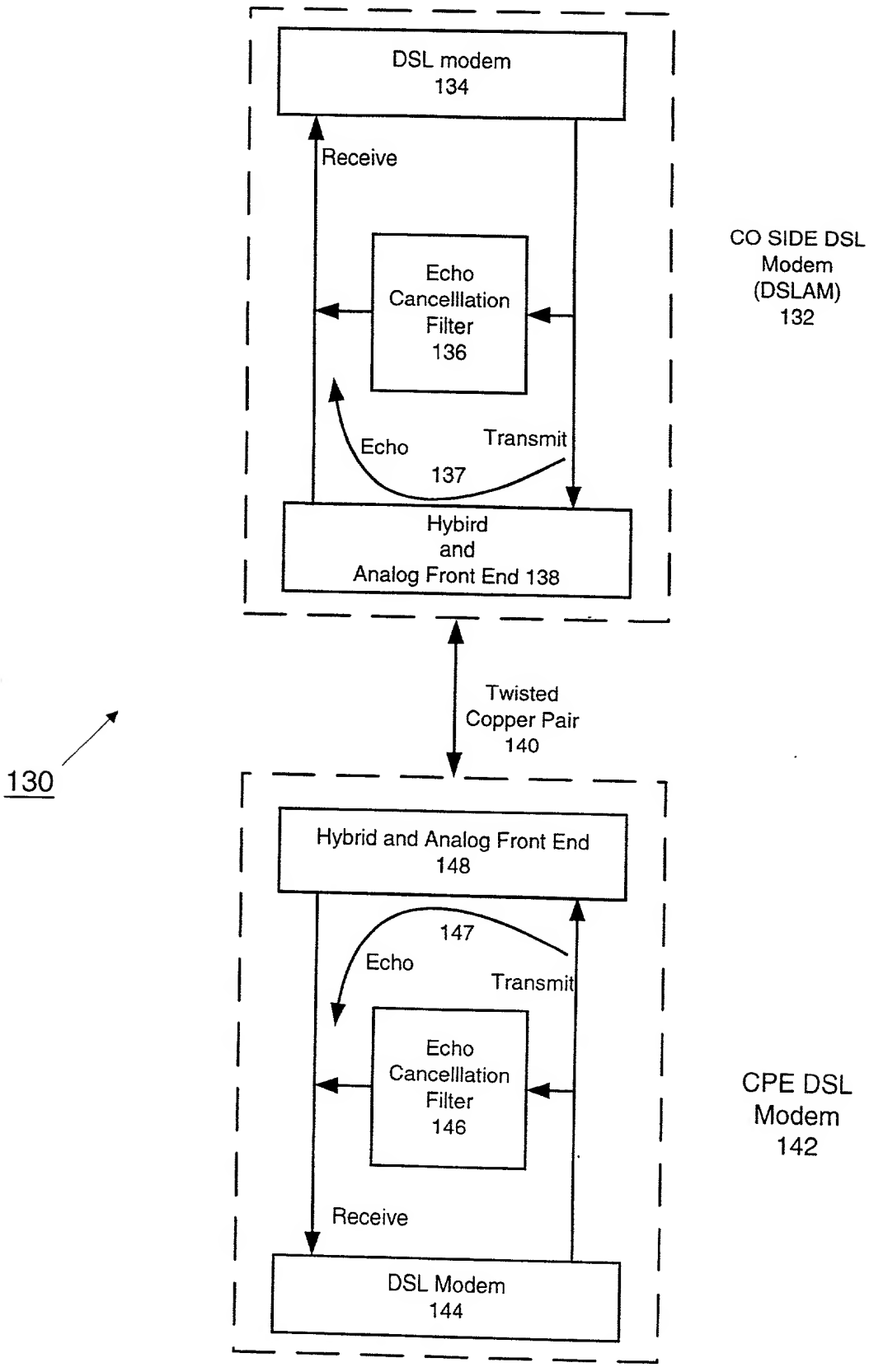

DSL modem
134
Receive
Echo
Cancelllation
Filter
136
Echo
Transmit
137
Hybird
and
Analog Front End 138
CO SIDE DSL
Modem
(DSLAM)
132
Twisted
Copper Pair
140
130
Hybrid and Analog Front End
148
147
Echo
Transmit
Echo
Cancelllation
Filter
146
Receive
DSL Modem
144
CPE DSL
Modem
142

FIG. 1b

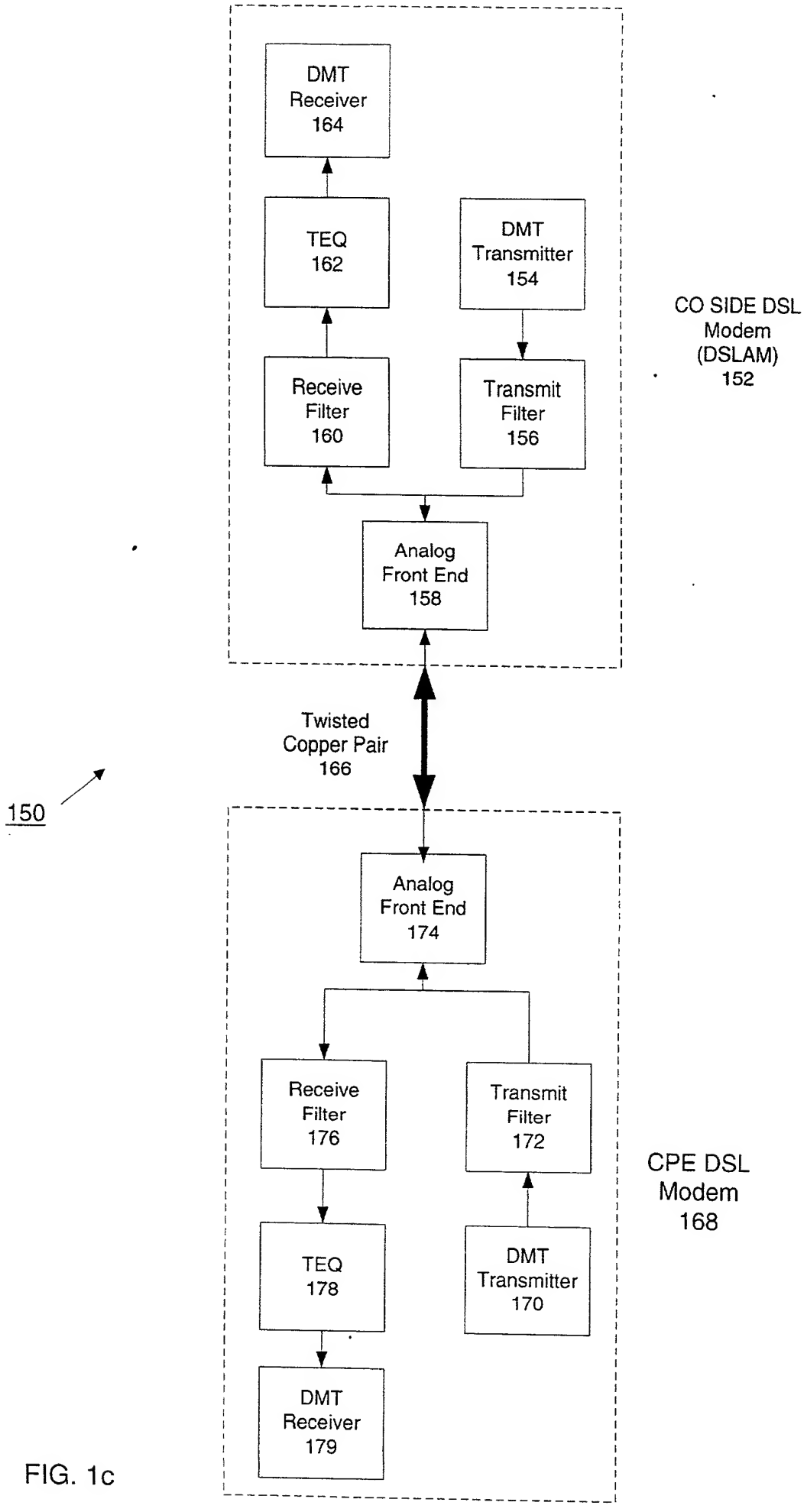

DMT Receiver 164
TEQ 162
DMT Transmitter 154
Receive Filter 160
Transmit Filter 156
Analog Front End 158
CO SIDE DSL Modem (DSLAM) 152
Twisted Copper Pair 166
150
Analog Front End 174
Receive Filter 176
Transmit Filter 172
TEQ 178
DMT Transmitter 170
DMT Receiver 179
CPE DSL Modem 168

FIG. 1c

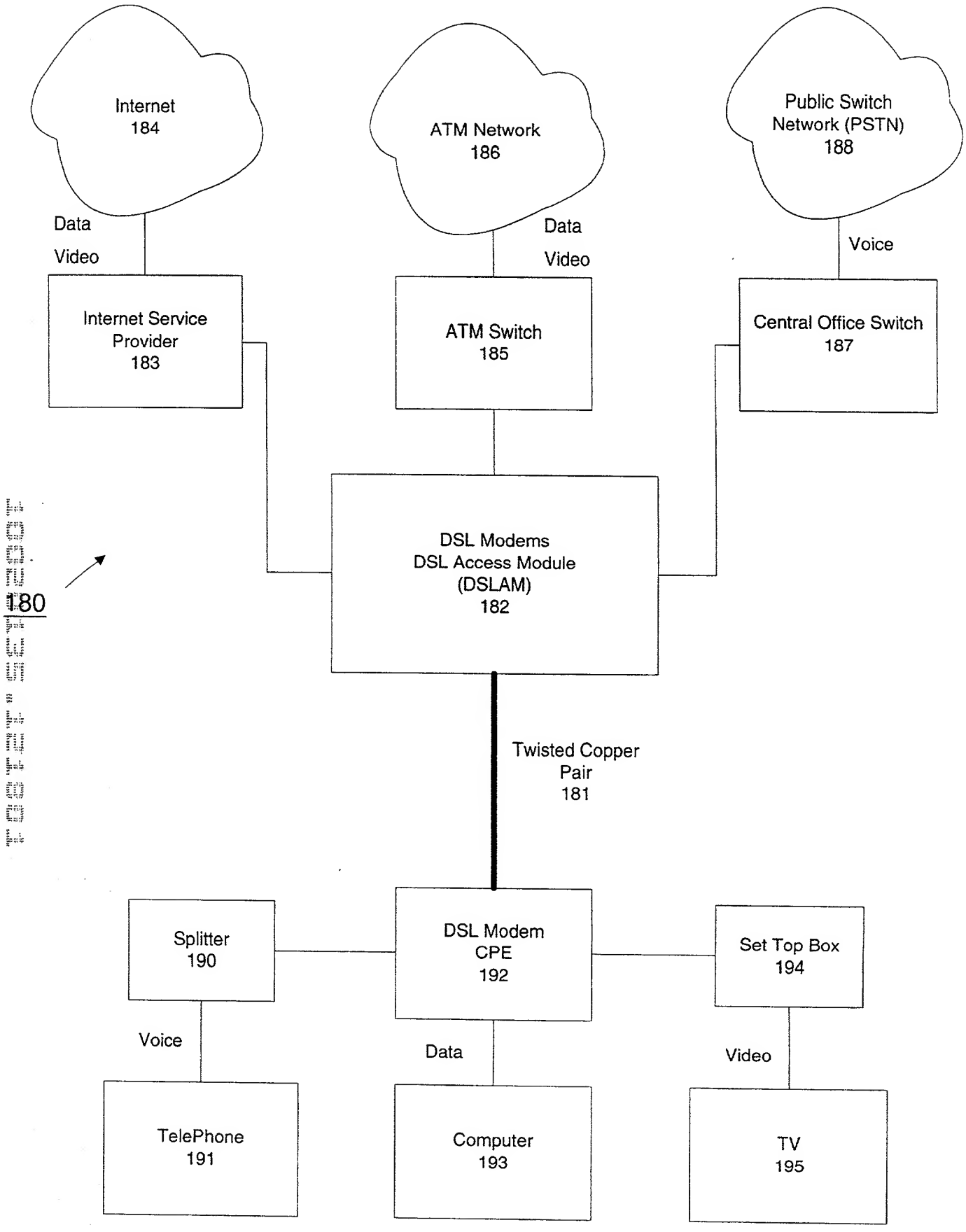

Internet
184
ATM Network
186
Public Switch
Network (PSTN)
188
Data
Video
Data
Video
Voice
Internet Service
Provider
183
ATM Switch
185
Central Office Switch
187
DSL Modems
DSL Access Module
(DSLAM)
182
180
Twisted Copper
Pair
181
Splitter
190
DSL Modem
CPE
192
Set Top Box
194
Voice
Data
Video
TelePhone
191
Computer
193
TV
195

FIG. 1d

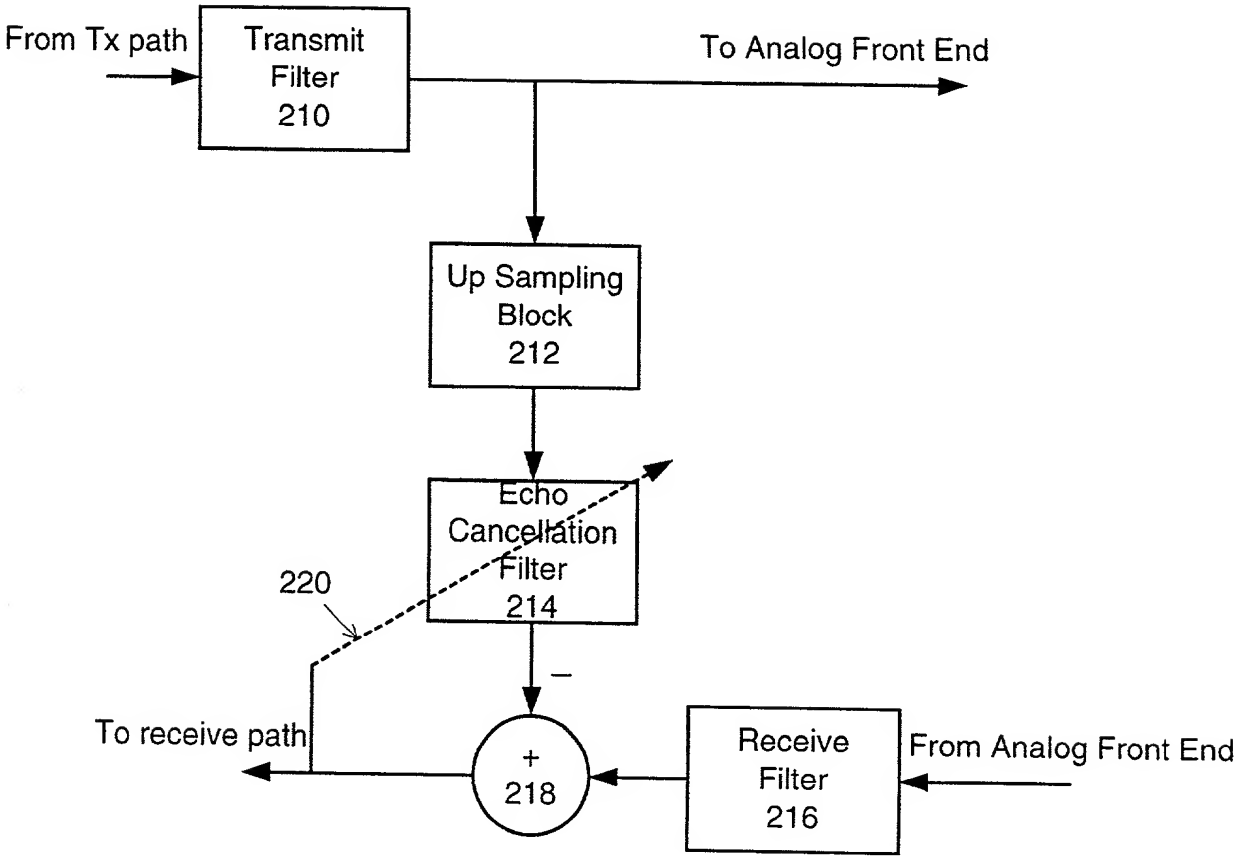

From Tx path
Transmit Filter 210
To Analog Front End
Up Sampling Block 212
Echo Cancellation Filter 214
220
To receive path
+ 218
Receive Filter 216
From Analog Front End

FIG. 2

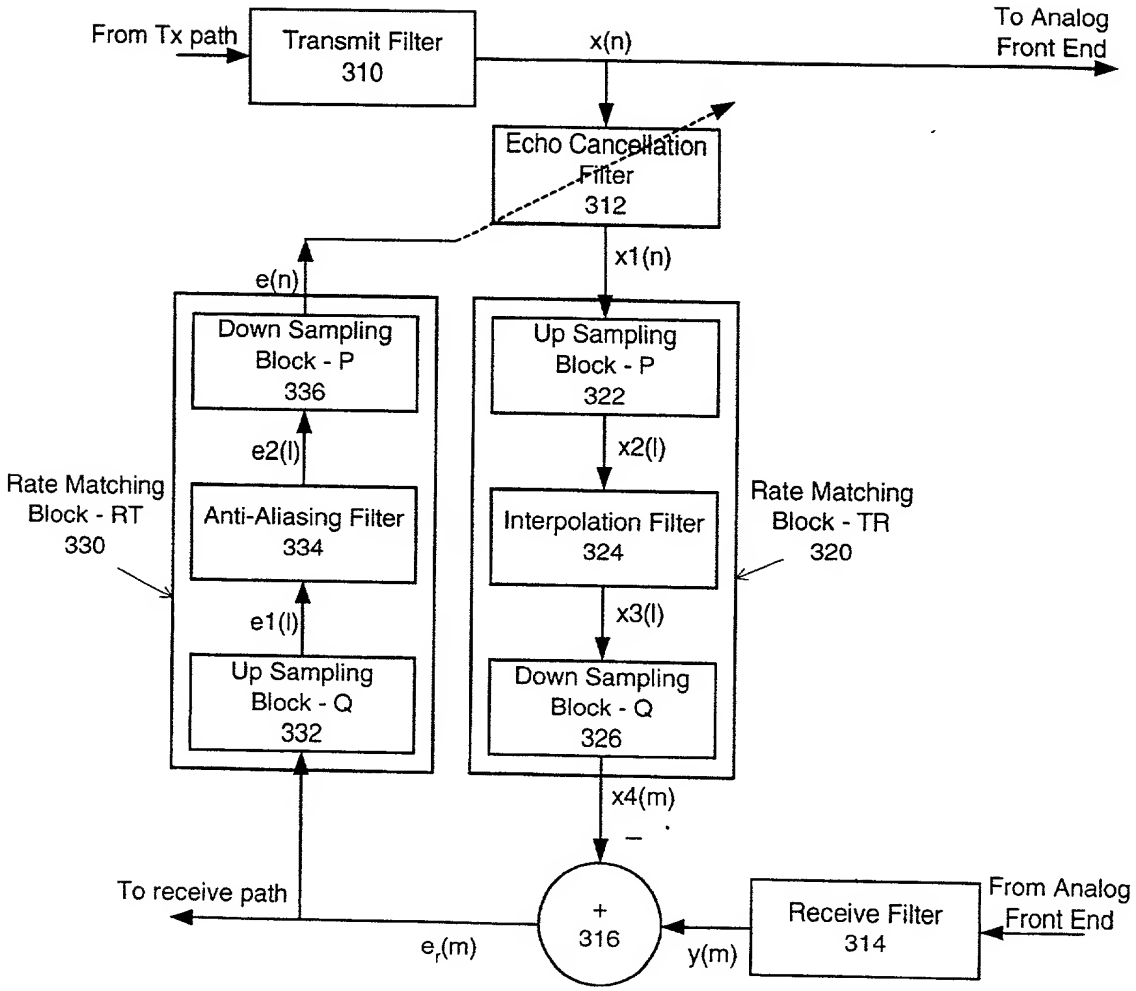

From Tx path
Transmit Filter
310
x(n)
To Analog
Front End
Echo Cancellation
Filter
312
x1(n)
e(n)
Down Sampling
Block - P
336
e2(l)
Anti-Aliasing Filter
334
e1(l)
Up Sampling
Block - Q
332
Rate Matching
Block - RT
330
Up Sampling
Block - P
322
x2(l)
Interpolation Filter
324
x3(l)
Down Sampling
Block - Q
326
Rate Matching
Block - TR
320
x4(m)
To receive path
+
316
−
Receive Filter
314
From Analog
Front End
$e_r(m)$
y(m)

FIG. 3

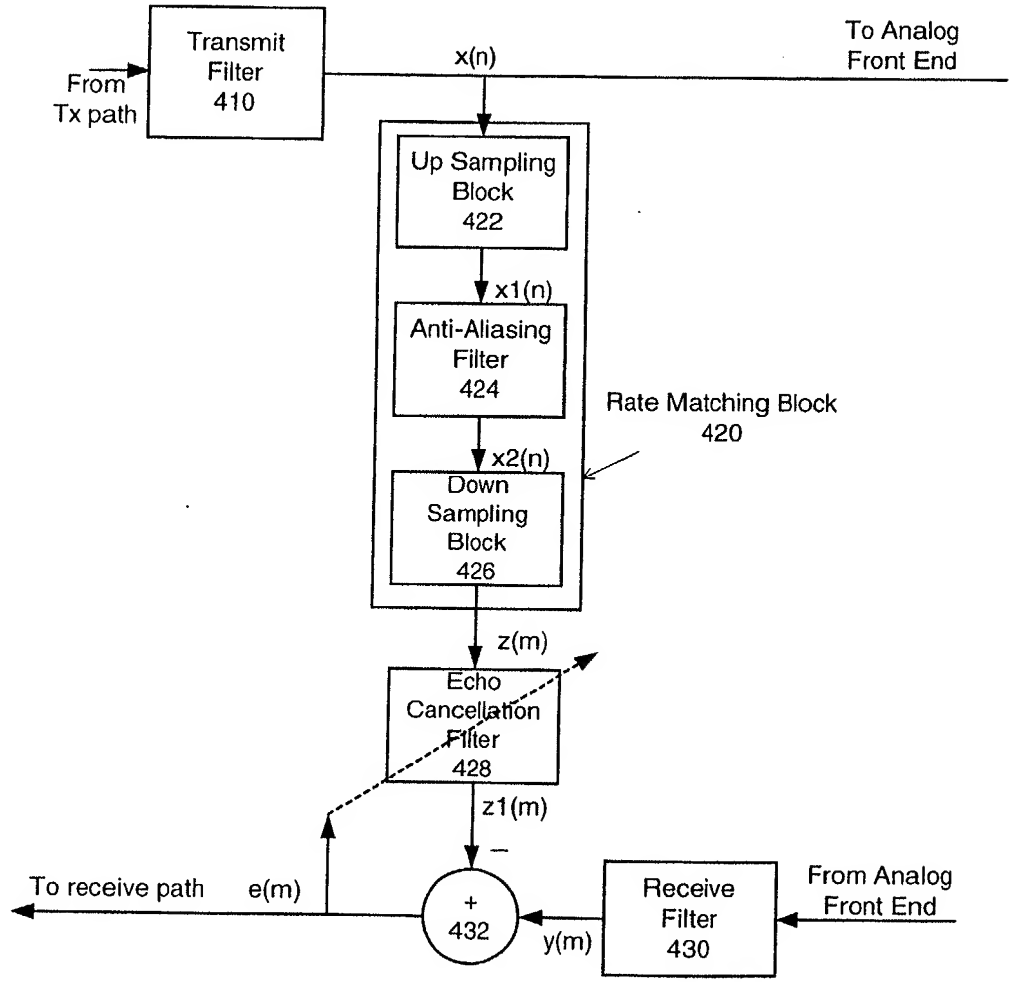

Transmit
Filter
410
From
Tx path
x(n)
To Analog
Front End
Up Sampling
Block
422
x1(n)
Anti-Aliasing
Filter
424
x2(n)
Down
Sampling
Block
426
Rate Matching Block
420
z(m)
Echo
Cancellation
Filter
428
z1(m)
–
+
432
y(m)
Receive
Filter
430
From Analog
Front End
To receive path
e(m)

FIG. 4

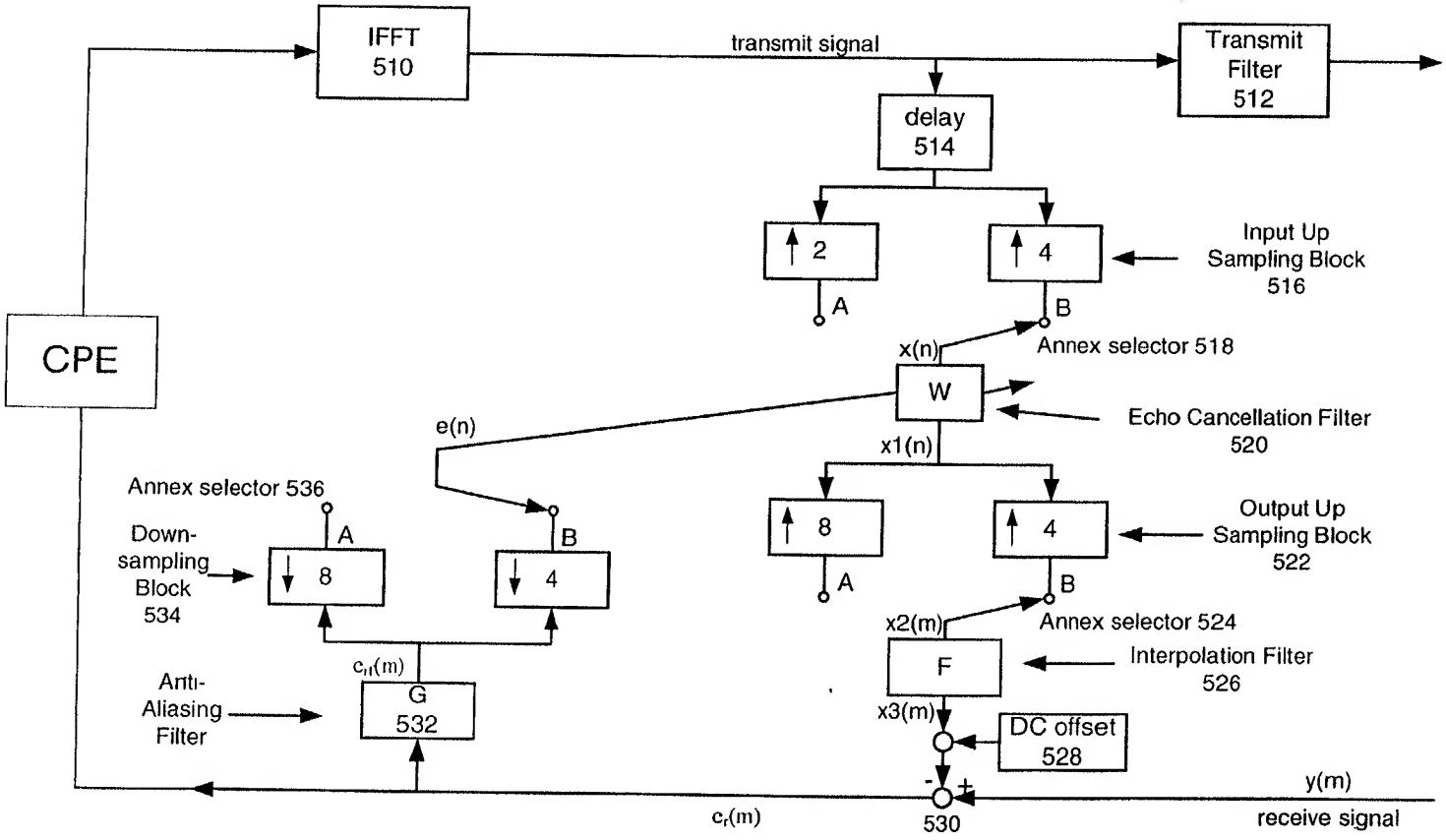


FIG. 5

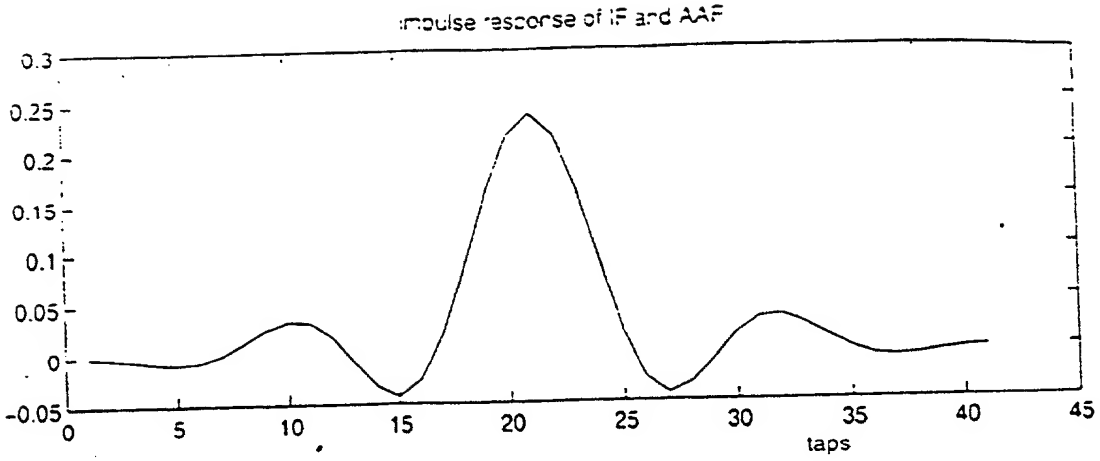


Figure 6

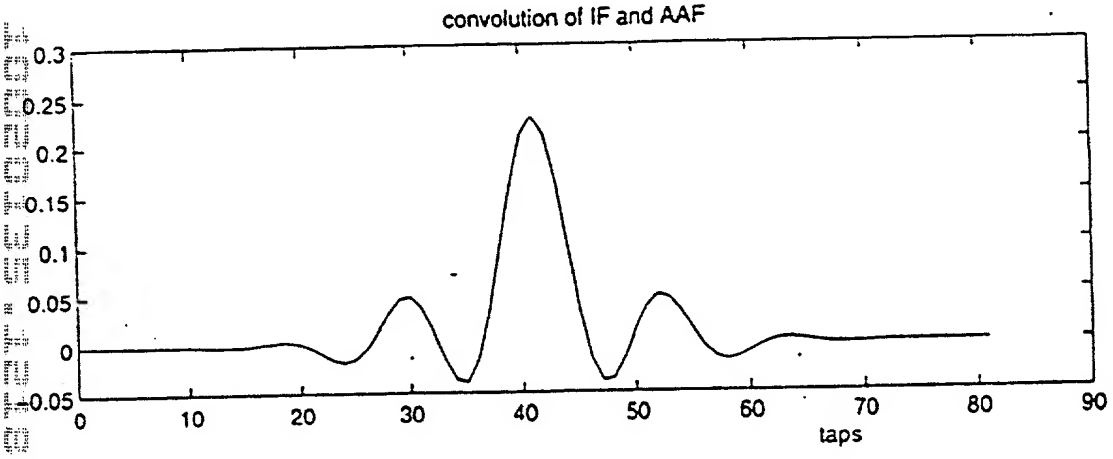


Figure 7

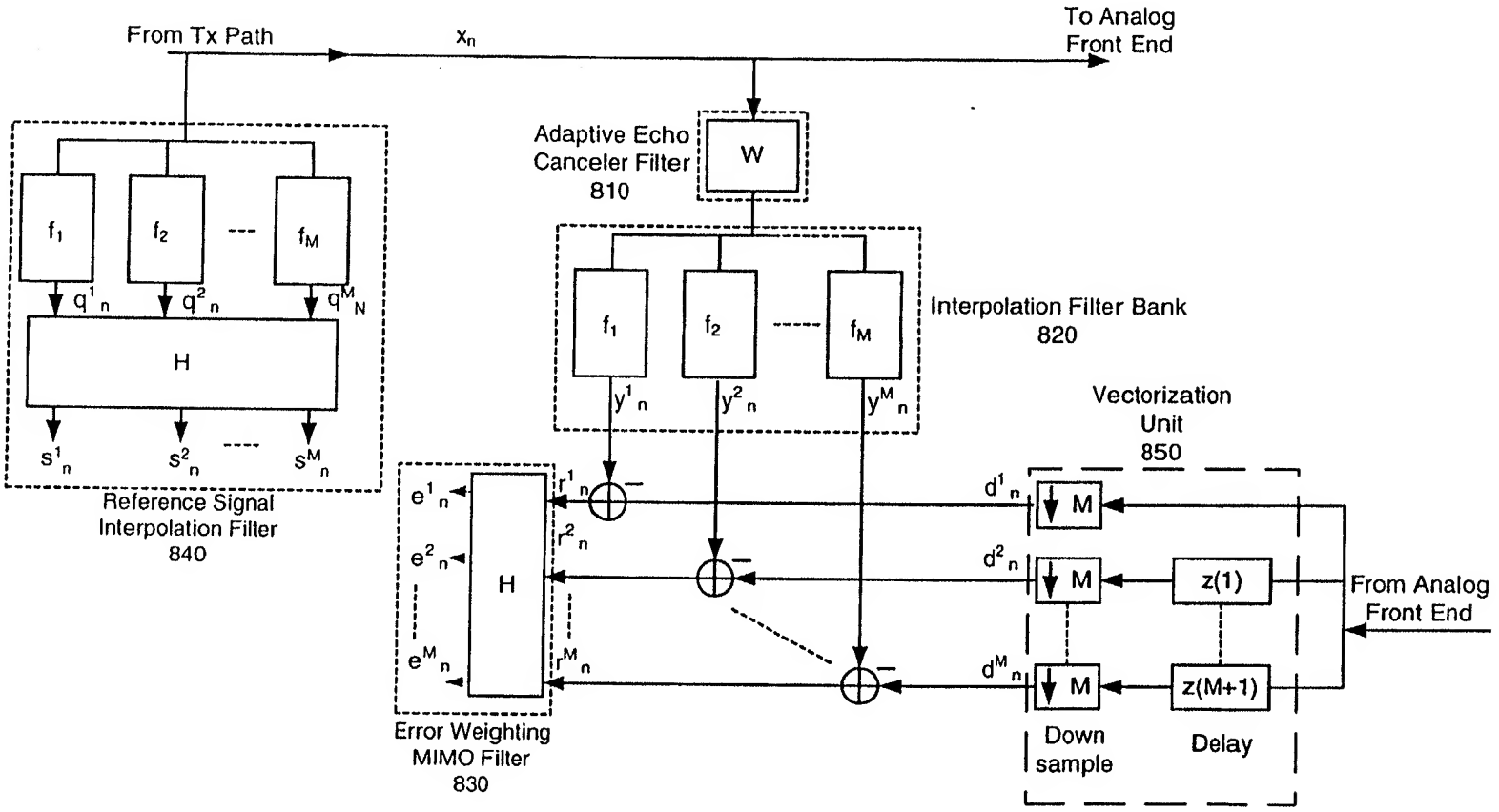


FIG. 8

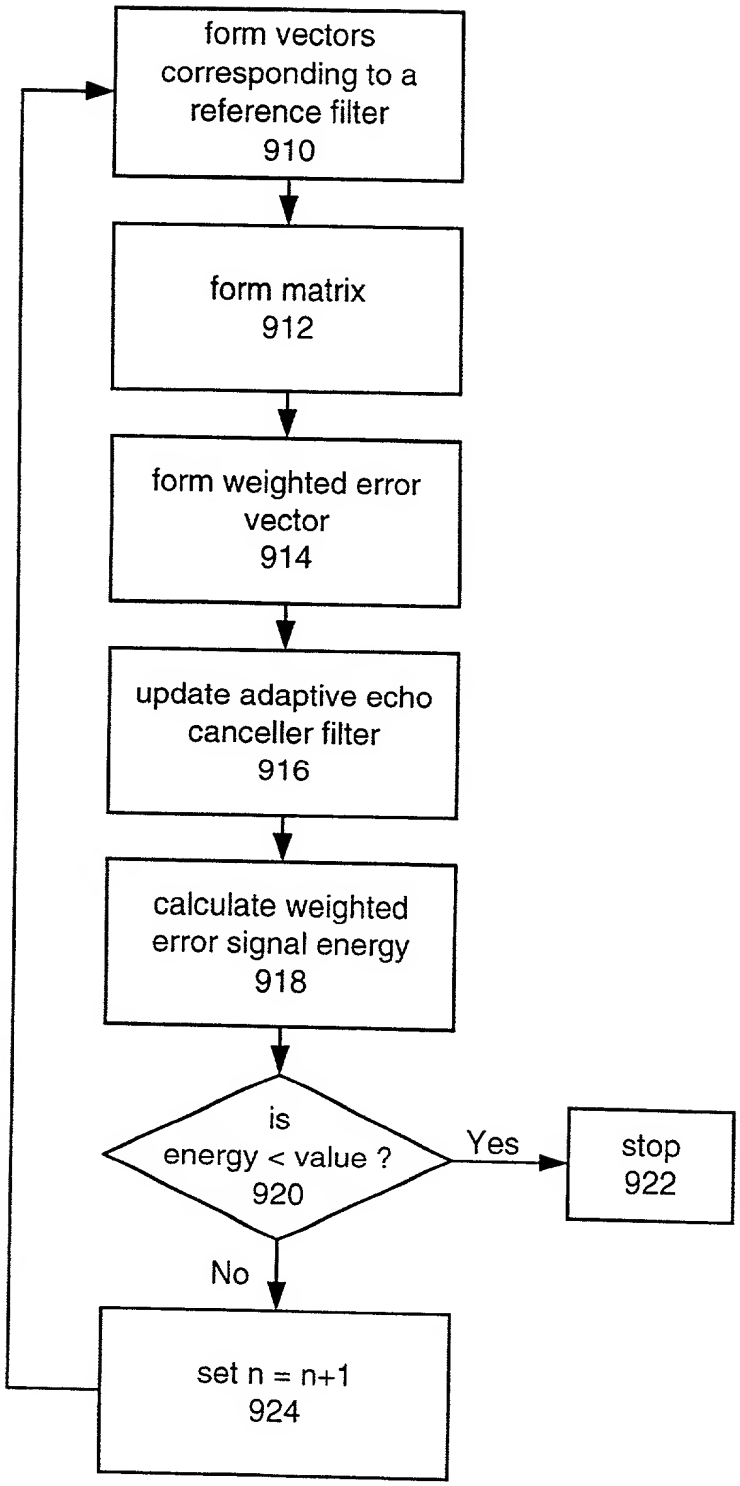

form vectors corresponding to a reference filter 910
form matrix 912
form weighted error vector 914
update adaptive echo canceller filter 916
calculate weighted error signal energy 918
is energy < value ? 920
Yes
stop 922
No
set n = n+1 924

FIG. 9

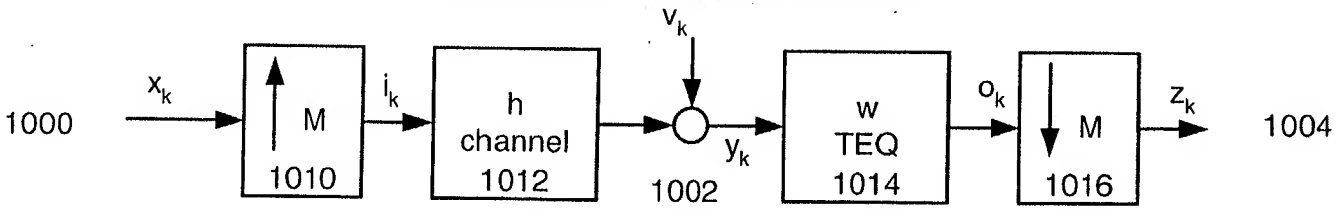


FIG. 10a

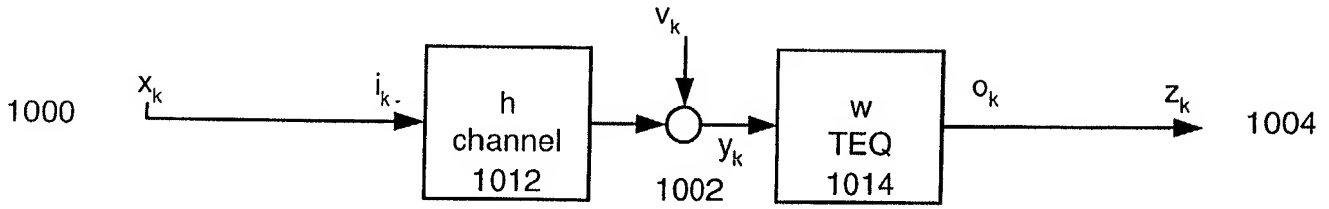
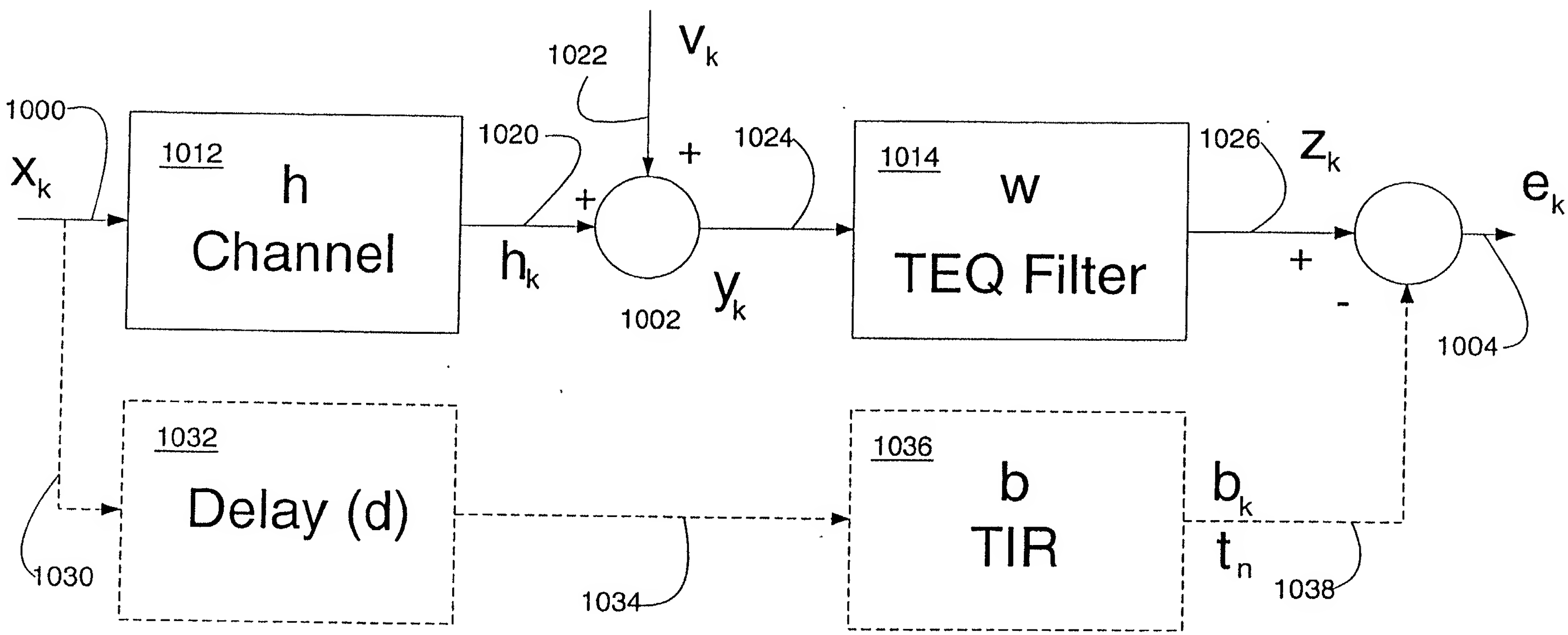


FIG. 10b



1000
x_k
1012
h
Channel
1020
h_k
1022
v_k
+
+
1002
1024
y_k
1014
w
TEQ Filter
1026
z_k
+
-
1004
e_k
1030
1032
Delay (d)
1034
1036
b
TIR
b_k
t_n
1038

Fig. 10c

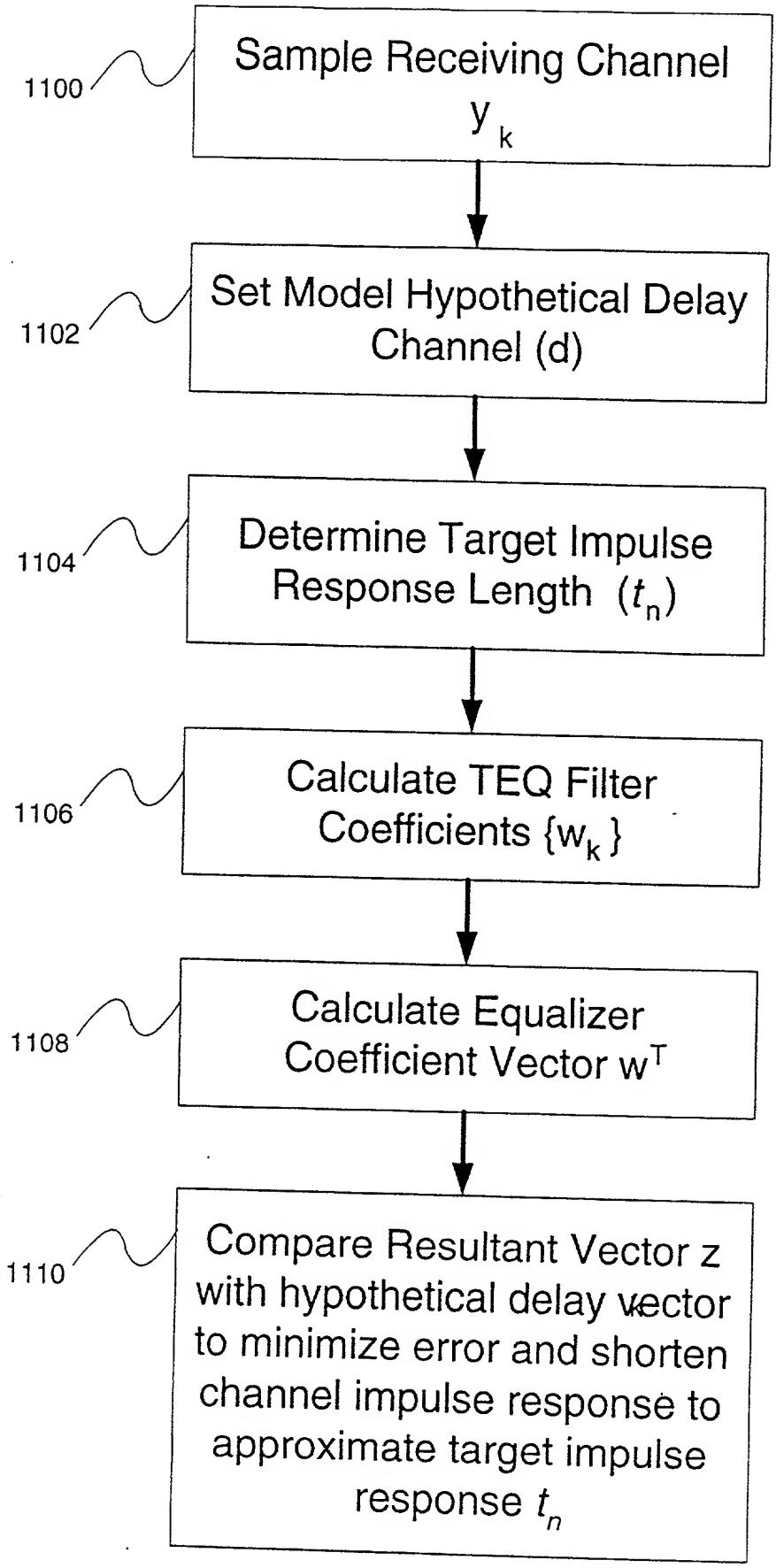

1100
Sample Receiving Channel y_k
1102
Set Model Hypothetical Delay Channel (d)
1104
Determine Target Impulse Response Length (t_n)
1106
Calculate TEQ Filter Coefficients $\{w_k\}$
1108
Calculate Equalizer Coefficient Vector w^T
1110
Compare Resultant Vector z with hypothetical delay vector to minimize error and shorten channel impulse response to approximate target impulse response t_n

Fig. 11

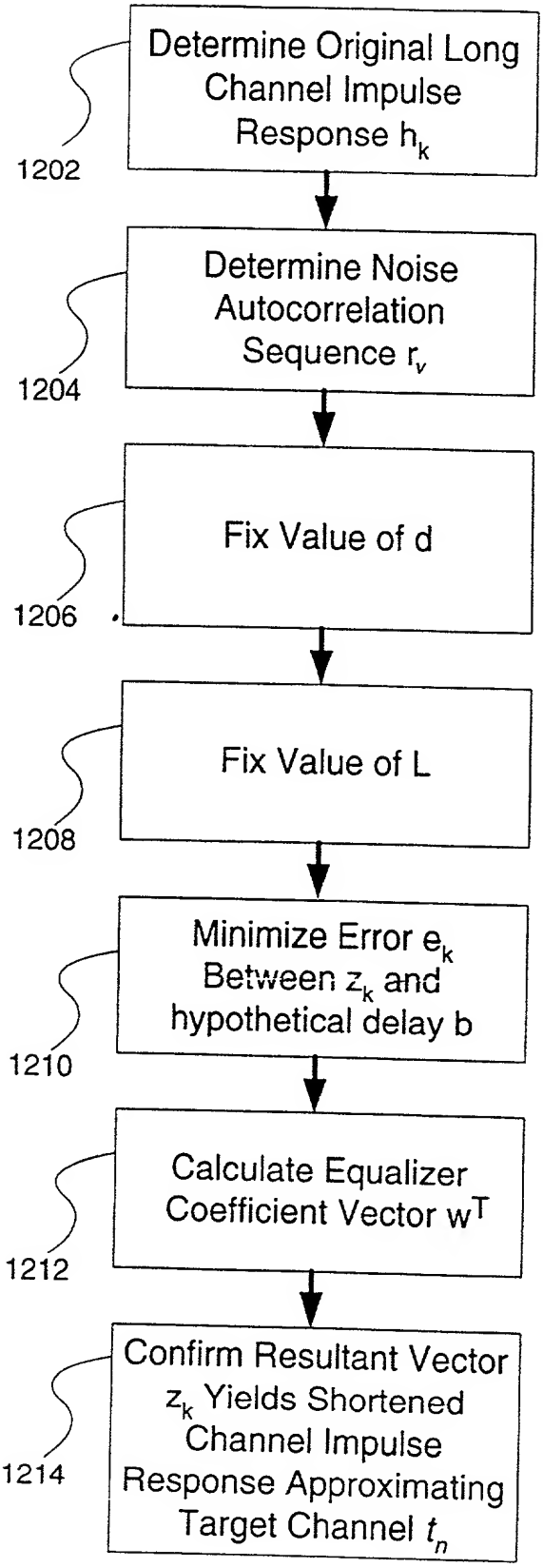

Determine Original Long Channel Impulse Response h_k
1202
Determine Noise Autocorrelation Sequence r_v
1204
Fix Value of d
1206
Fix Value of L
1208
Minimize Error e_k Between z_k and hypothetical delay b
1210
Calculate Equalizer Coefficient Vector w^T
1212
Confirm Resultant Vector z_k Yields Shortened Channel Impulse Response Approximating Target Channel t_n
1214

Fig. 12

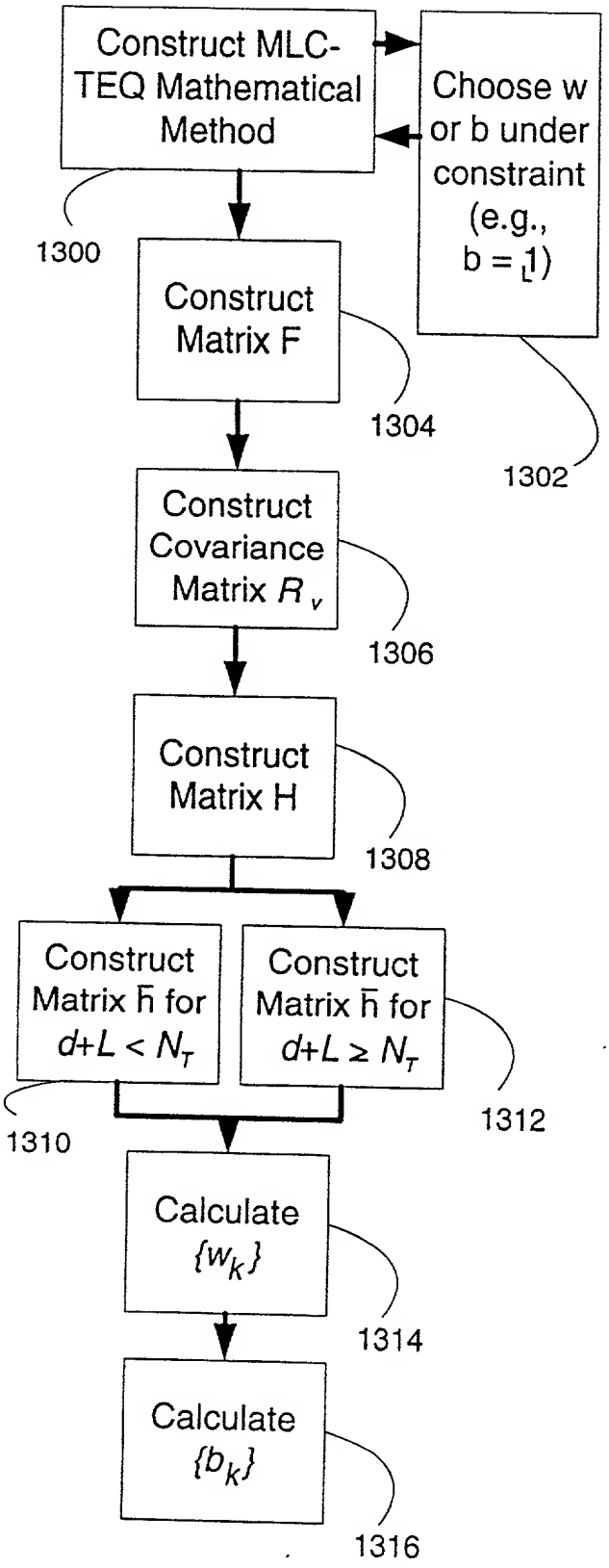

Construct MLC-TEQ Mathematical Method
Choose w or b under constraint (e.g., b = 1)
1300
Construct Matrix F
1304
1302
Construct Covariance Matrix R_v
1306
Construct Matrix H
1308
Construct Matrix $\bar{h}$ for $d+L < N_T$
Construct Matrix $\bar{h}$ for $d+L \geq N_T$
1310
1312
Calculate $\{w_k\}$
1314
Calculate $\{b_k\}$
1316

Fig. 13

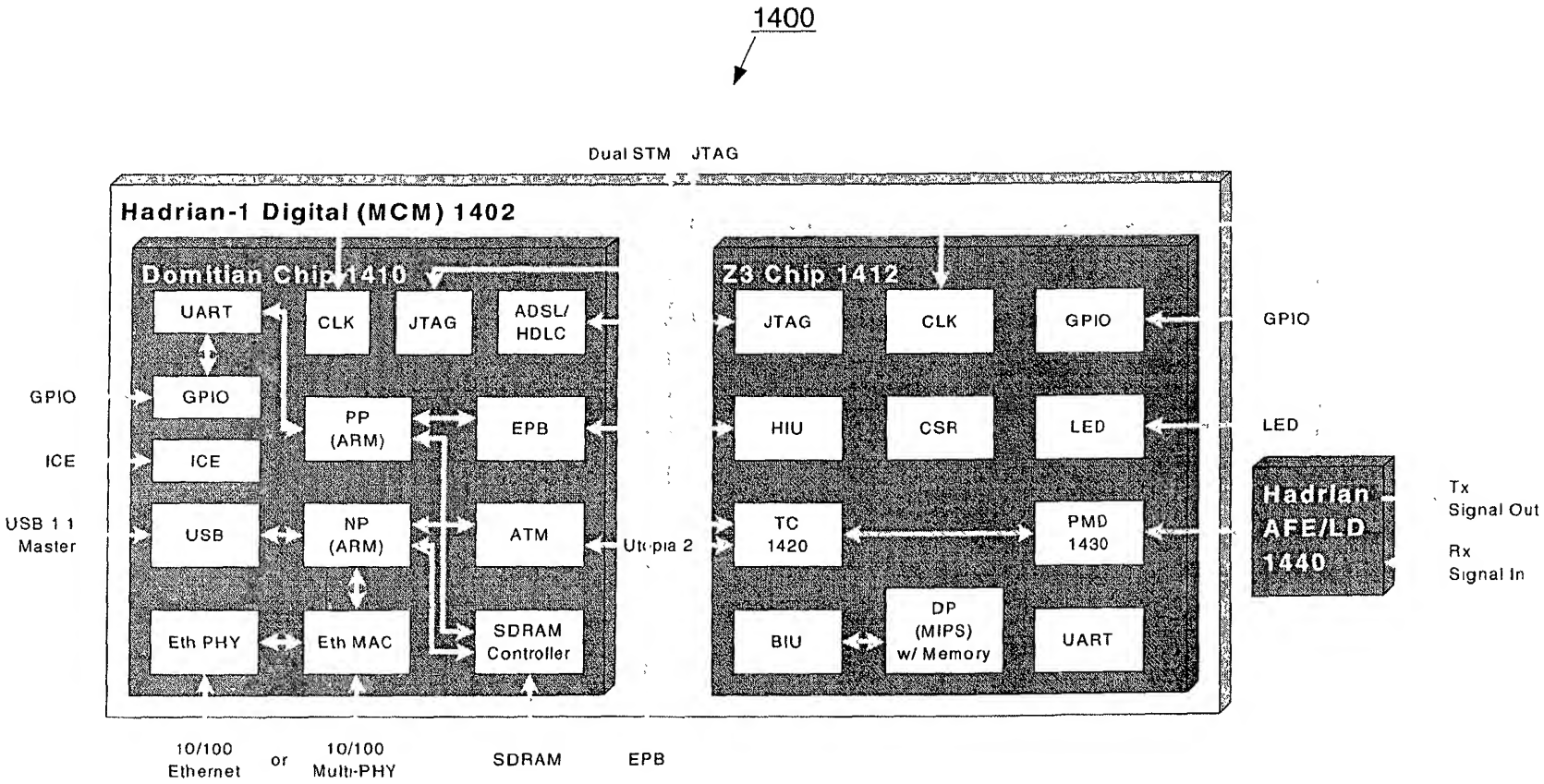


FIG. 14a

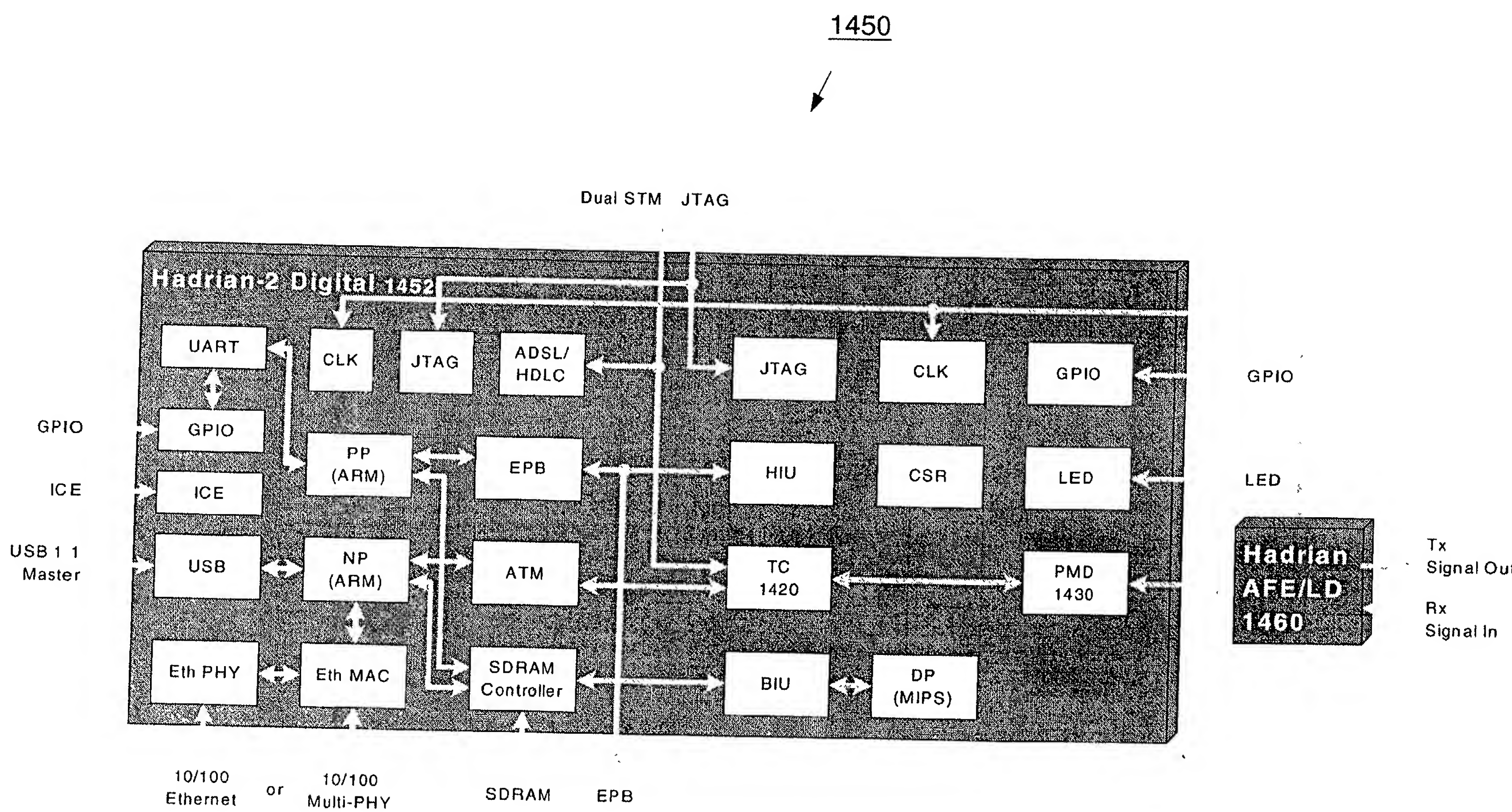

1450
Dual STM
JTAG
Hadrian-2 Digital 1452
UART
CLK
JTAG
ADSL/
HDLC
JTAG
CLK
GPIO
GPIO
GPIO
PP
(ARM)
EPB
HIU
CSR
LED
LED
ICE
ICE
USB 1 1
Master
USB
NP
(ARM)
ATM
TC
1420
PMD
1430
Hadrian
AFE/LD
1460
Tx
Signal Out
Rx
Signal In
Eth PHY
Eth MAC
SDRAM
Controller
BIU
DP
(MIPS)
10/100
Ethernet
or
10/100
Multi-PHY
SDRAM
EPB

FIG. 14b

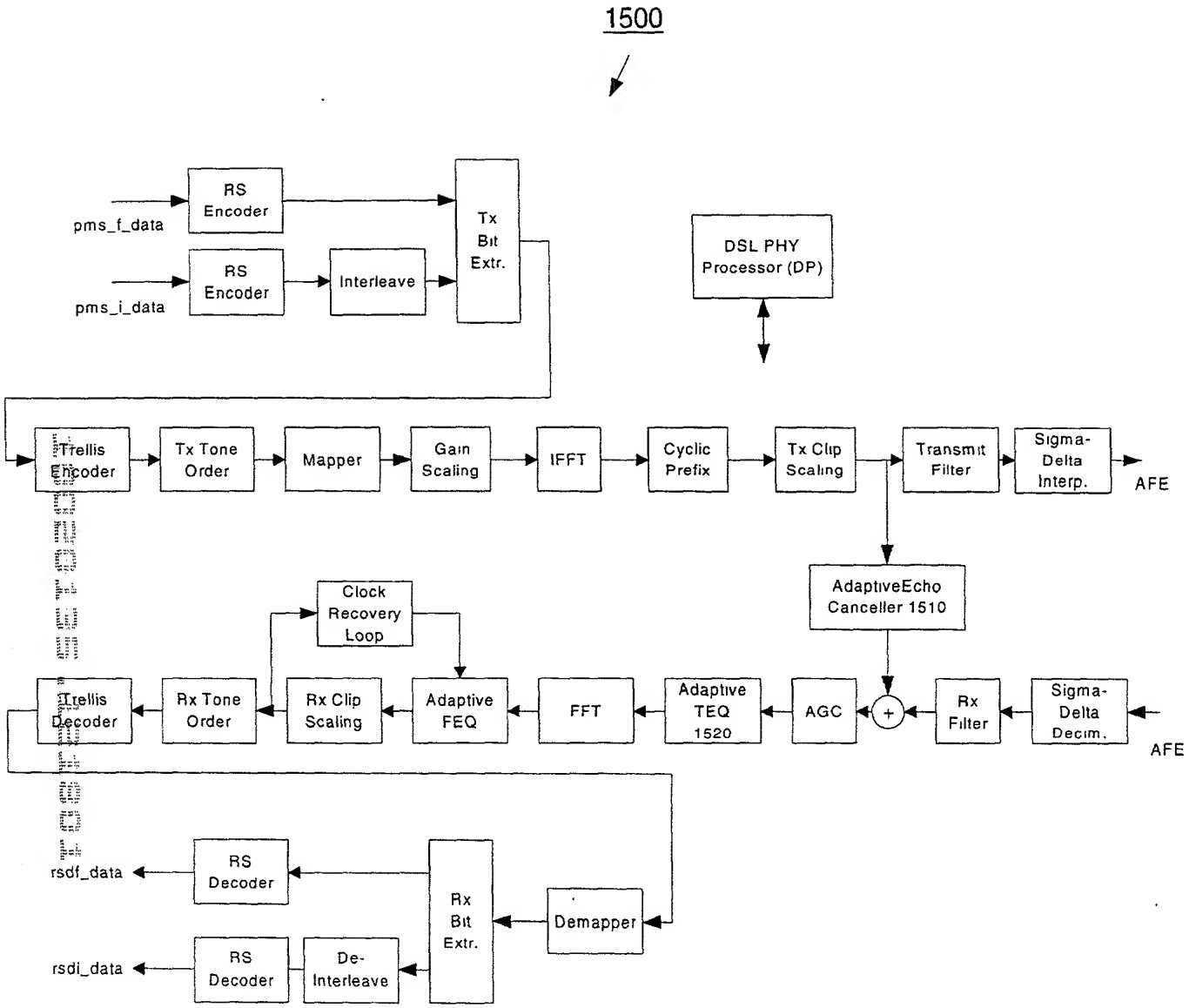

1500
RS Encoder
pms_f_data
RS Encoder
pms_i_data
Interleave
Tx Bit Extr.
DSL PHY Processor (DP)
Trellis Encoder
Tx Tone Order
Mapper
Gain Scaling
IFFT
Cyclic Prefix
Tx Clip Scaling
Transmit Filter
Sigma-Delta Interp.
AFE
AdaptiveEcho Canceller 1510
Clock Recovery Loop
Trellis Decoder
Rx Tone Order
Rx Clip Scaling
Adaptive FEQ
FFT
Adaptive TEQ 1520
AGC
Rx Filter
Sigma-Delta Decim.
AFE
RS Decoder
rsdf_data
RS Decoder
rsdi_data
De-Interleave
Rx Bit Extr.
Demapper

FIG. 15

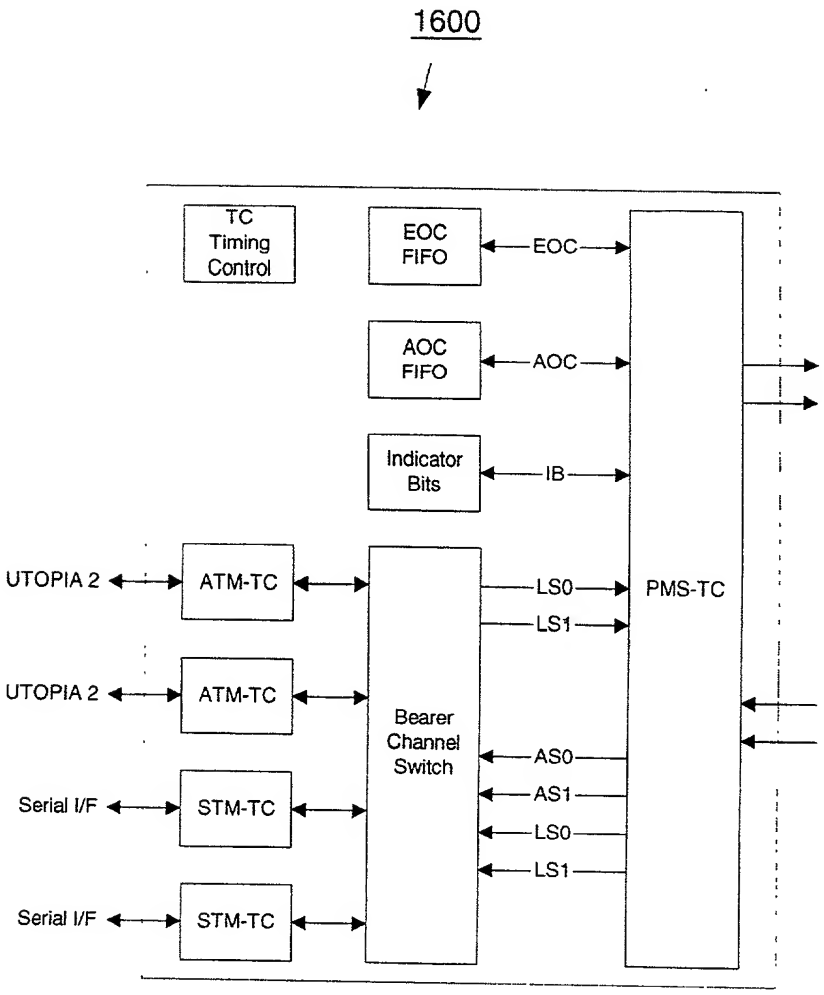

1600
TC Timing Control
EOC FIFO
EOC
AOC FIFO
AOC
Indicator Bits
IB
UTOPIA 2
ATM-TC
UTOPIA 2
ATM-TC
Serial I/F
STM-TC
Serial I/F
STM-TC
Bearer Channel Switch
LS0
LS1
AS0
AS1
LS0
LS1
PMS-TC

FIG. 16

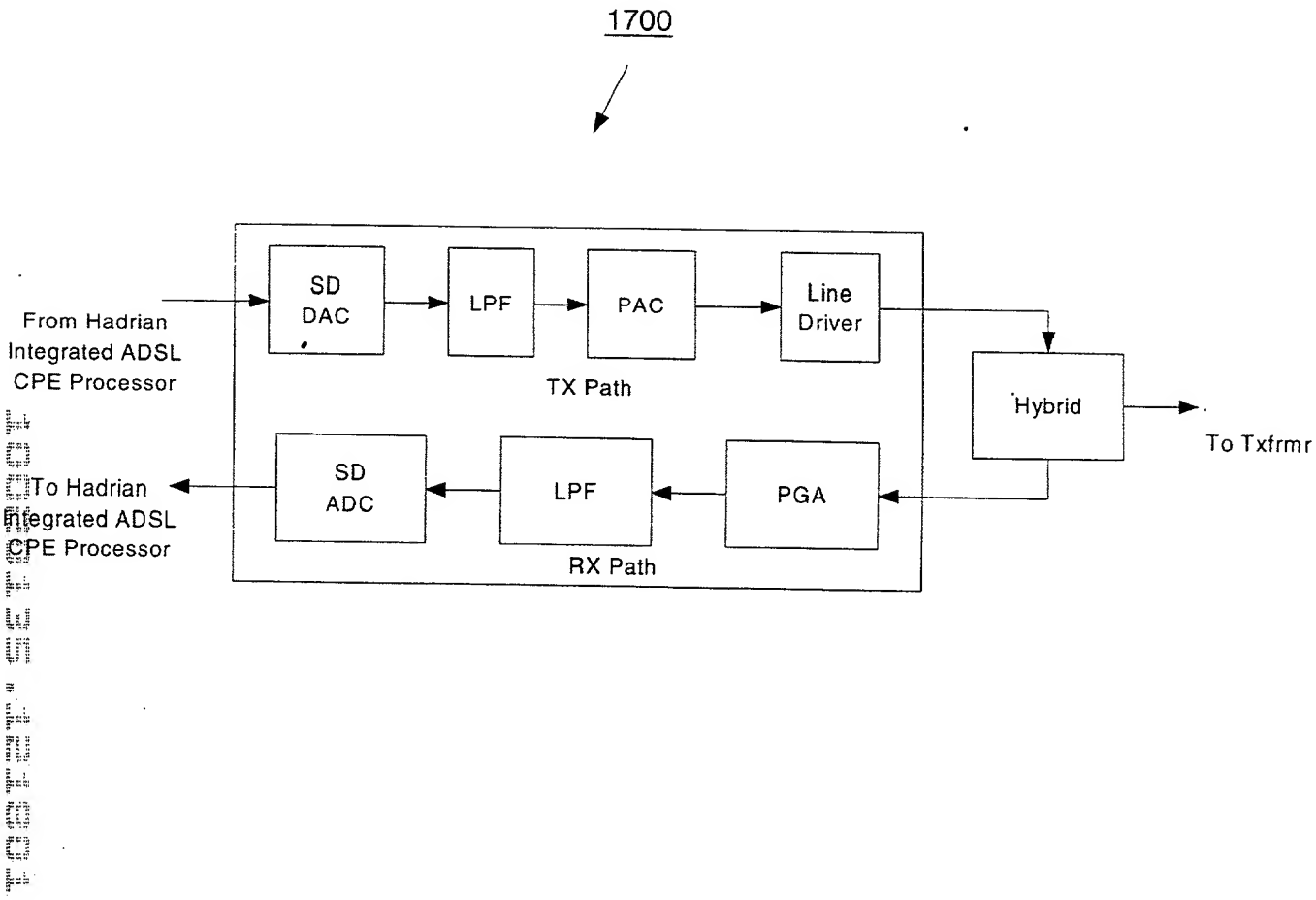

1700
From Hadrian Integrated ADSL CPE Processor
SD DAC
LPF
PAC
Line Driver
TX Path
Hybrid
To Txfrmr
To Hadrian Integrated ADSL CPE Processor
SD ADC
LPF
PGA
RX Path

FIG. 17

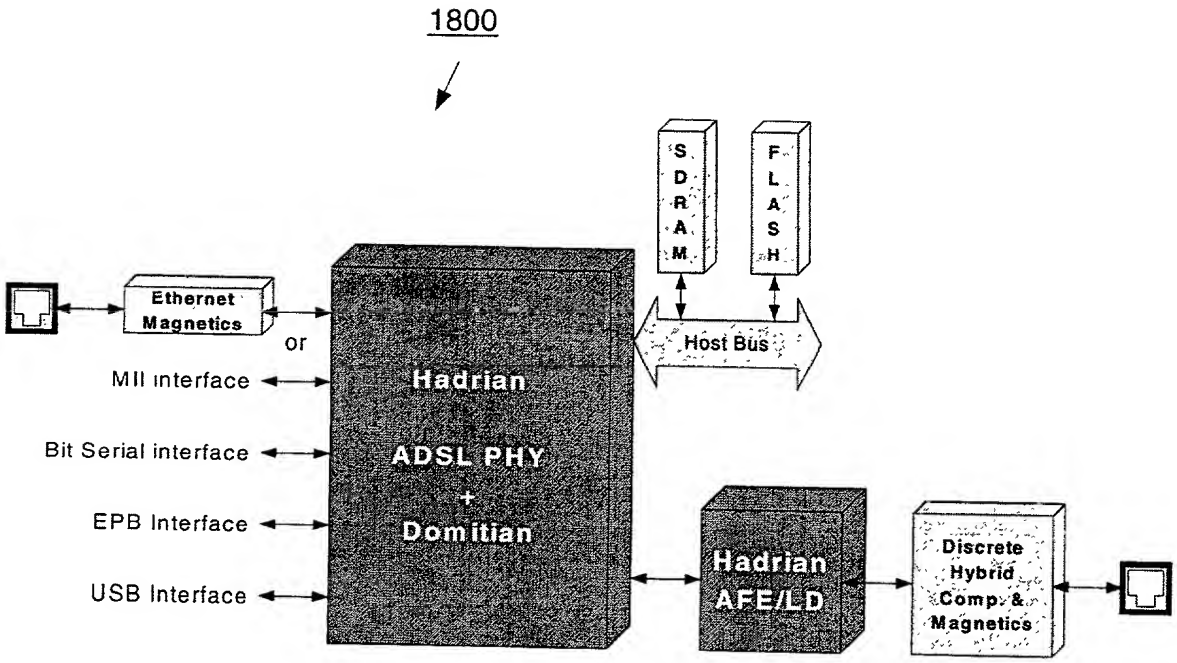

1800
S D R A M
F L A S H
Ethernet Magnetics
or
MII interface
Bit Serial interface
EPB Interface
USB Interface
Hadrian
ADSL PHY
+
Domitian
Host Bus
Hadrian AFE/LD
Discrete Hybrid Comp. & Magnetics

FIG. 18a

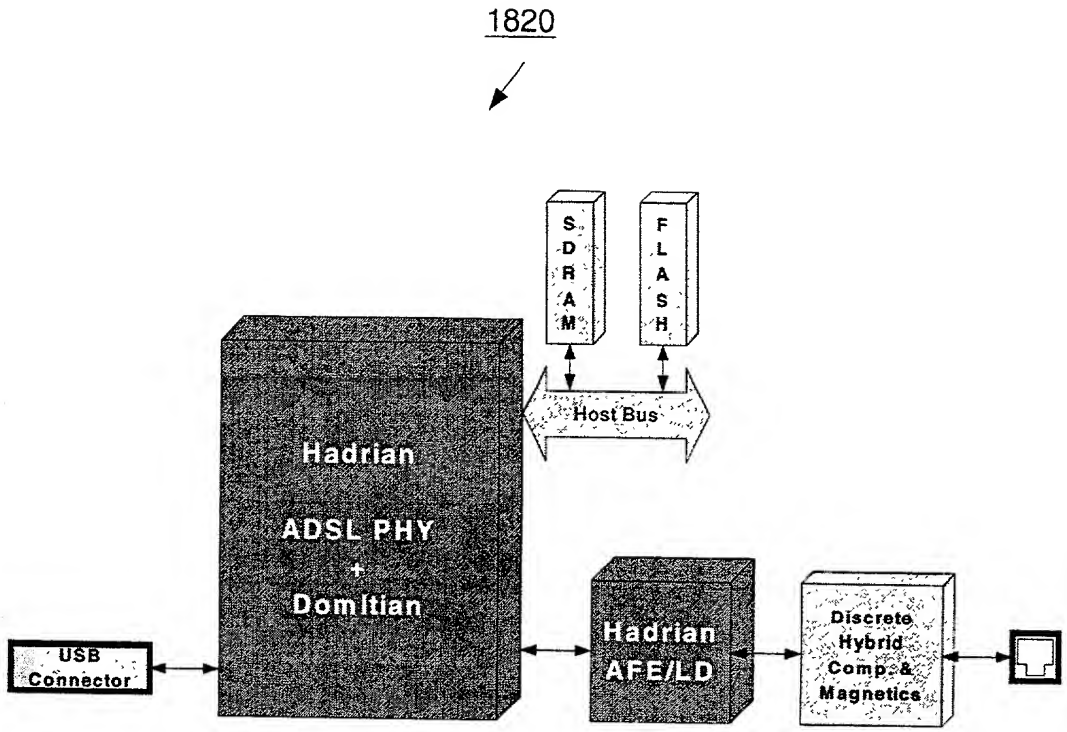

1820
SDRAM
FLASH
Host Bus
Hadrian
ADSL PHY
+
DomItian
USB
Connector
Hadrian
AFE/LD
Discrete
Hybrid
Comp. &
Magnetics

FIG. 18b

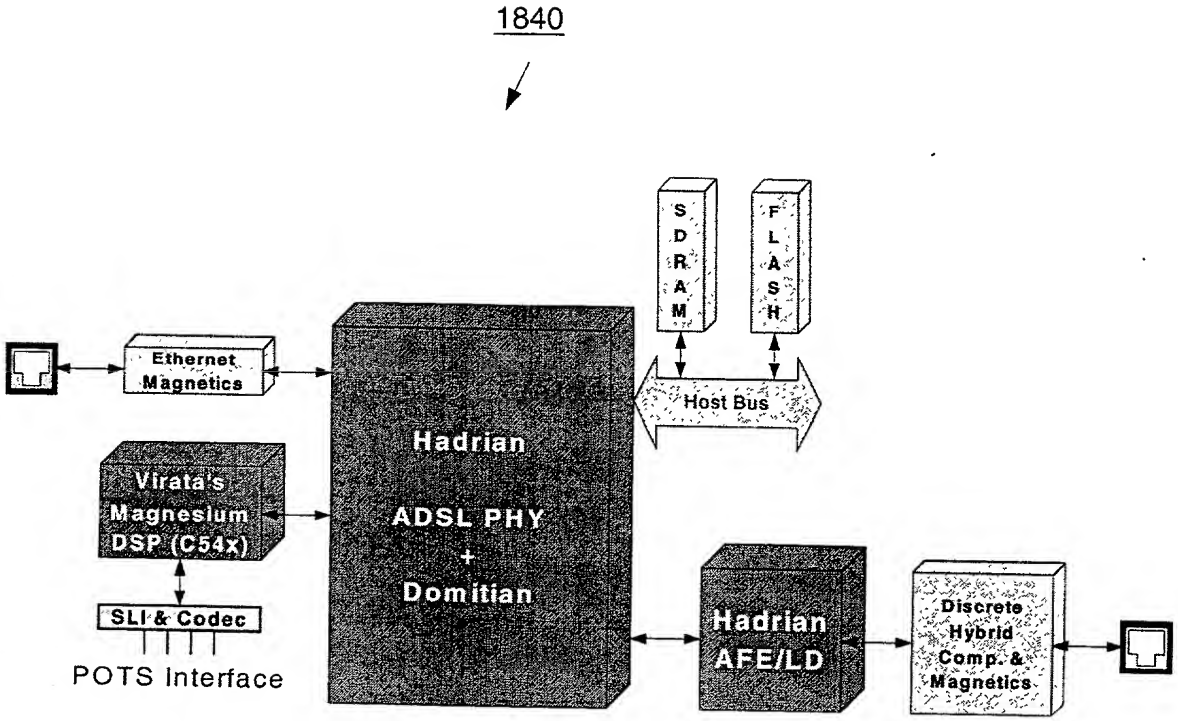

1840
S
D
R
A
M
F
L
A
S
H
Ethernet
Magnetics
Host Bus
Hadrian
ADSL PHY
+
Domitian
Virata's
Magnesium
DSP (C54x)
SLI & Codec
POTS Interface
Hadrian
AFE/LD
Discrete
Hybrid
Comp. &
Magnetics

FIG. 18c